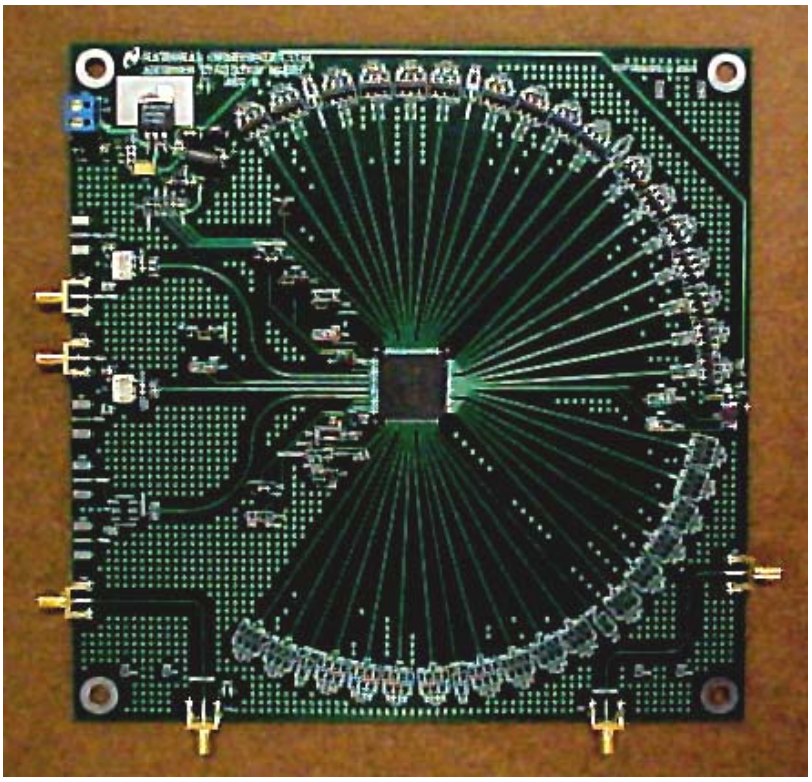
National Semiconductor

July 13, 2005
Revision B

Evaluation Board Instruction Manual

ADC08D1500 - Dual 8-Bit, 1.5 GSPS, 1.8W A/D Converter



ADC08D1500EVAL BOARD USER MANUAL – TABLE OF CONTENTS

1.0 Introduction

The ADC08D1500EVAL Board is designed to allow quick evaluation and design-in of National Semiconductor's ADC08D1500 8-bit Analog-to-Digital Converter. This device is specified for 1.5 GSPS operation.

This board is NOT designed to function with National Semiconductor's WaveVision™ Capture Board, but is intended for data capture with an appropriate Logic Analyzer, such as the Agilent 16702B. The digitized (8 bit) output is available at the headers placed around the board. The data and associated clock is provided in differential LVDS format.

Once data has been acquired by the Logic Analyzer, it can be saved as an ASCII text file and analyzed with an FFT software package, such as Matlab or National Semiconductor's WaveVision software.

2.0 Board Assembly

The ADC08D1500 Evaluation Board is assembled with balun-connected transformers (T1,T2 & T3) to convert the single-ended clock and analog inputs to differential signals. The ADC08D1500 device is configured through an internal pull down resistor to accept differential signals from the transformer outputs.

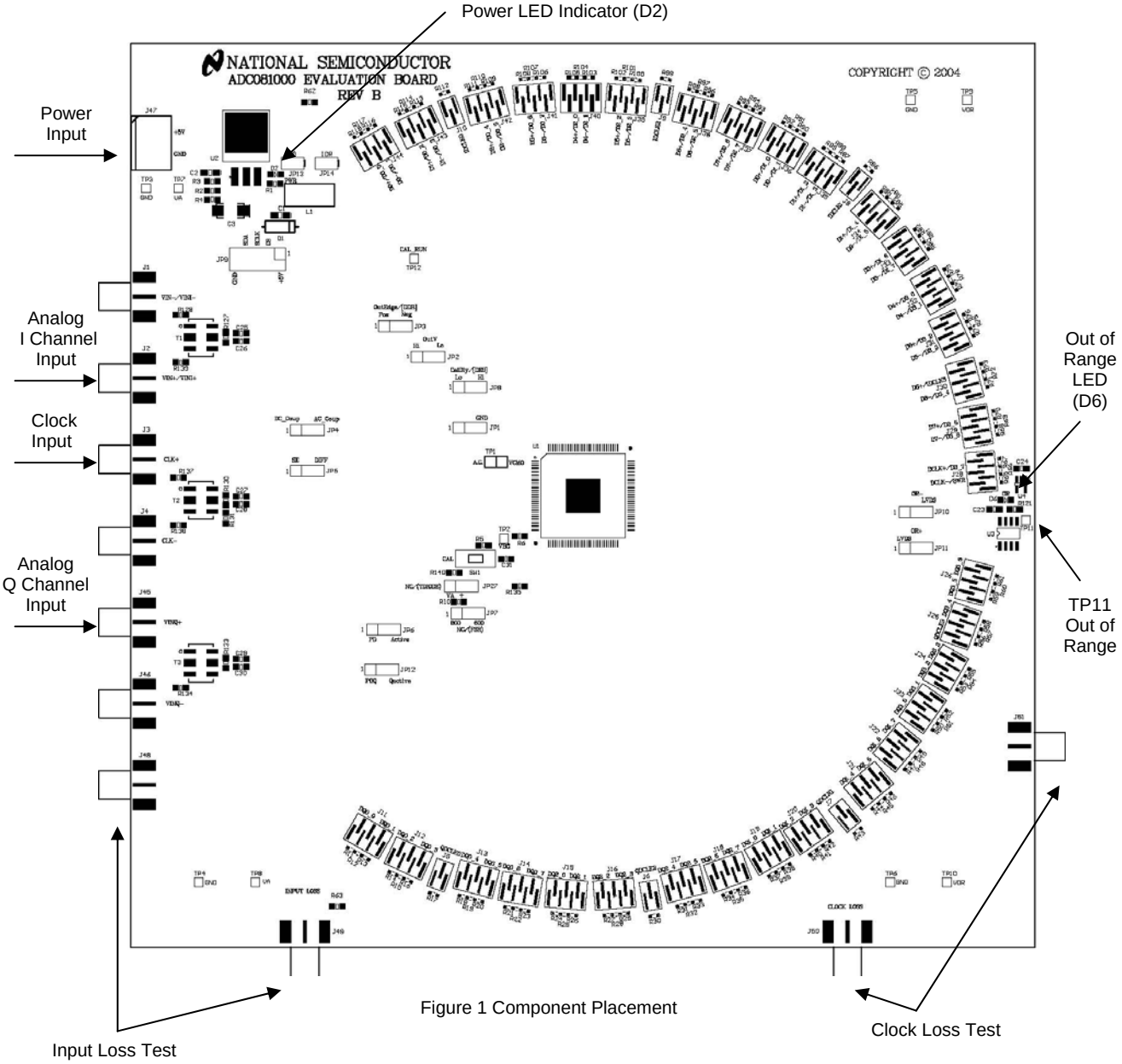


Figure 1 Component Placement

3.0 Quick Start

Refer to Figure 1 for locations of test points and major components.

For Stand-Alone operation:

1. Connect a 4.5V to 5.0V d.c. power source to Power Connector J47. This supply should be capable of delivering 1 Amp.
2. Connect a stable signal source capable of supplying a 1.5 GHz clock signal at 0dBm, such as the Rhode & Schwarz SME-03, to SMA connector J3.
3. Connect a stable sine wave source capable of supplying the desired input frequencies at up to 8 dBm. Connect this signal to SMA connector J2 through a band pass filter. The exact level needed from the generator will depend upon the insertion loss of the filter used.
4. Be sure that all jumpers are in the default position as shown in Table 3 Section 10.
5. Connect the Logic Analyzer flying leads to the differential signal pins on the headers.
6. Turn on the power to the board. Turn on the clock and analog input signal sources.
7. Set the clock source to 200 MHz at 0 dBm.
8. Set the signal source for the analog input to 8 dBm at the desired frequency. Observe the ‘Out of Range’ LED (D6) at the end of the board opposite the input SMA connectors. If this LED is not on, increase the input signal source until it is.
9. Reduce the input level until the ‘Out of Range’ LED just turns off.
10. Set the clock source to the desired sample rate and acquire data using the logic analyzer.

4.0 Functional Description

The ADC08D1500 Evaluation Board schematic is shown in Section 8.0.

4.1 Input circuitry

The input signal(s) to be digitized should be applied to SMA connectors J2 and/or J45. These 50 Ohm inputs are intended to accept a low-noise sine wave signal. To accurately evaluate the dynamic performance of this converter, the input test signals will have to be passed through a high-quality bandpass filter with at least 10-bit equivalent noise and distortion characteristics.

Signal transformers T1 and T3, are connected as baluns, and provide single-ended to differential conversion. The differential PCB traces to the ADC analog input pins have a characteristic differential impedance of 100 Ohms.

No scope or other test equipment should be connected anywhere in the signal path while gathering data.

This evaluation board as delivered is set up for operation with two single-ended analog inputs, which are converted to differential signals. If it is desired to connect an external differential signal source to this board, transformer T1 and T3 should be removed and pins 1 and 6 of their pads should be shorted together, as should pins 3 and 4. Remove R128 (near J1) and R134 (near J46) and install an SMA connector at J1 and J46 for the inverted signal inputs.

4.2 ADC reference

The ADC08D1500 has an internal reference that can not be adjusted. However, the Full-Scale (differential) Range may be selected to be either 800 mV P-P or 600 mV P-P with jumper JP4 Refer to Table 3 in Section 10 for further information on Jumper Settings.

4.3 ADC clock

The clock signal applied to the ADC is applied to SMA Connector J3. The board is set by default for a single-ended clock. The balun-transformer (T2) converts the single ended clock source to a differential signal to drive the ADC clock pins. If it is desired to use a differential clock source, T2 should be removed and pins 1 and 6 of its pad should be shorted together, as should pins 3 and 4. Remove the resistor R138 and install a SMA connector at J4 for the inverted clock input.

Note that it is very important that the ADC clock should be as free of jitter as possible or apparent SNR of the ADC08D1500 will be compromised.

4.4 Digital Data Output

The 2 channel digital output data from the ADC08D1500 is available at the thirty two 7-pin header connectors (J11 to J44) on the board. J29 to J44 are connected to the I-Channel Outputs. J11 to J26 are connected to the Q-Channel Outputs These signal lines are connected to pins 3 and 5 of the headers and are differential LVDS in nature. The differential levels can be reduced by moving the jumper at JP2 to the "Lo" position. With lower levels there is less power consumption. However, noise immunity is decreased with the lower signal swing.

4.5 Power Requirements

The power supply requirement for the ADC08D1500 Evaluation Board is 4.5 V to 5.0V at 1.2 Amps.

The voltage regulator U2 will run warm to hot, so it is advised to keep the supply at the low end of the input range.

The board typically draws around 1.0A but it is always good practice to have extra power reserve in the power supply over the typical power requirements.

4.6 Power Supply Connections

Power to this board is supplied through power connector J47. The supply voltage to the board is protected against reverse polarity by a shunt diode.

The ADC08D1500 supply voltage can be measured at TP7 and TP8 and should be 1.9V, ±50 mV. The output driver supply voltage for the ADC08D1500 can be measured at TP9 and TP10 and should be the same potential as that measured at TP7 and TP8.

5.0 Installing the ADC08D1500 Evaluation Board

The evaluation board requires power supplies as described in Section 4.5, above.

An appropriate signal source should be connected to the Analog Inputs SMA J2 and J45. When evaluating dynamic performance, an appropriate signal generator (such as the HP8644B or the R&S SME-03 or SML-03) with 50 Ohm source impedance should be connected to the Analog Input BNC J2 and/or J45 through an appropriate band pass filter.

6.0 Obtaining Best Results

Obtaining the best results with any ADC requires both good circuit techniques and a good PC board layout. The layout has been optimized with the design of this evaluation board.

6.1 Clock Jitter

When any circuitry is added after a signal source, some jitter is almost always added to that signal. Jitter in a clock signal, depending upon how bad it is, can degrade dynamic performance. We can see the effects of jitter in the frequency domain (FFT) as "leakage" or "spreading" around the input frequency, as seen in Figure 2a. Compare this with the more desirable plot of Figure 2b. Note that all dynamic performance parameters (shown to the right of the FFT) are improved by eliminating clock jitter.

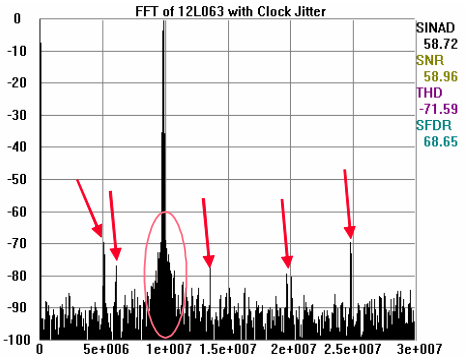


Figure 2a. Jitter causes a spreading around the input signal, as well as undesirable signal spurs.

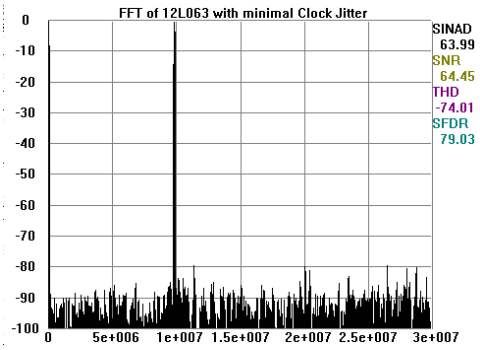


Figure 2b. Eliminating or minimizing clock jitter results in a more desirable FFT that is more representative of how the ADC actually performs.

6.2 Coherent Sampling

Artifacts can result when we perform an FFT on a digitized waveform, producing inconsistent results when testing repeatedly. The presence of these artifacts means that the ADC under test may perform better than the measurements would indicate.

We can eliminate the need for windowing and get more consistent results if we observe the proper ratios between the input and sampling frequencies. We call this coherent sampling. Coherent sampling greatly increases the spectral resolution of the FFT, allowing us to more accurately evaluate the spectral response of the A/D converter. When we do this, however, we must be sure that the input signal has high spectral purity and stability and that the

sampling clock signal is extremely stable with minimal jitter.

Coherent sampling of a periodic waveform occurs when a prime integer number of cycles exists in the sample window. The relationship between the number of cycles sampled (CY), the number of samples taken (SS), the signal input frequency (fin) and the sample rate (fs), for coherent sampling, is

$$\frac{CY}{SS} = \frac{f_{in}}{f_s}$$

CY, the number of cycles in the data record, must be a prime integer number and SS, the number of samples in the data record, must be a factor of 2 integer.

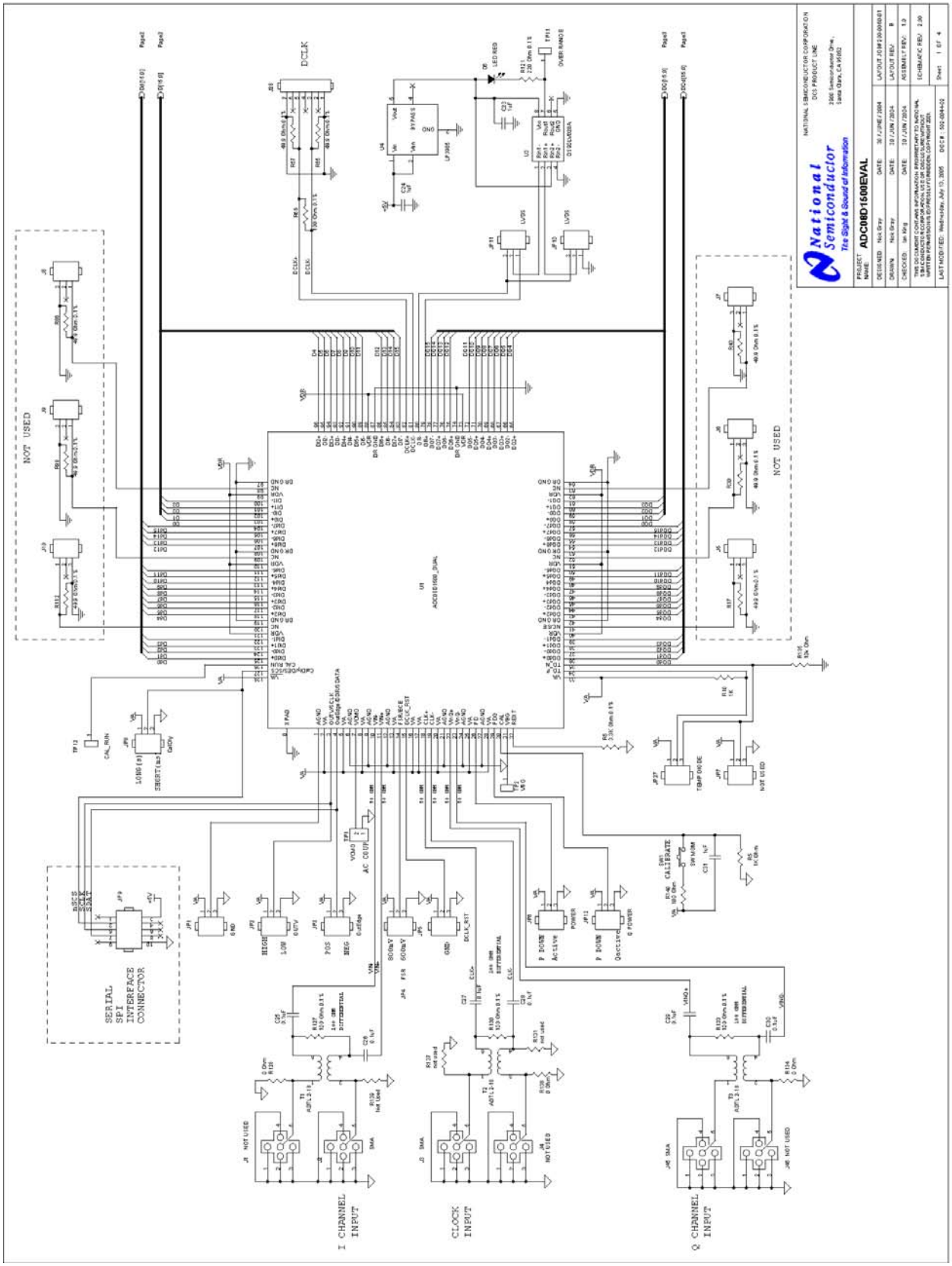
Further, f_{in} (signal input frequency) and f_s (sampling rate) should be locked to each other so that the relationship between the two frequencies is exact. Locking the two signal sources to each other also causes whatever sample-to-sample clock edge timing variation (jitter) that is present in the two signals to cancel each other.

Windowing (an FFT Option under WaveVision™) should be turned off for coherent sampling.

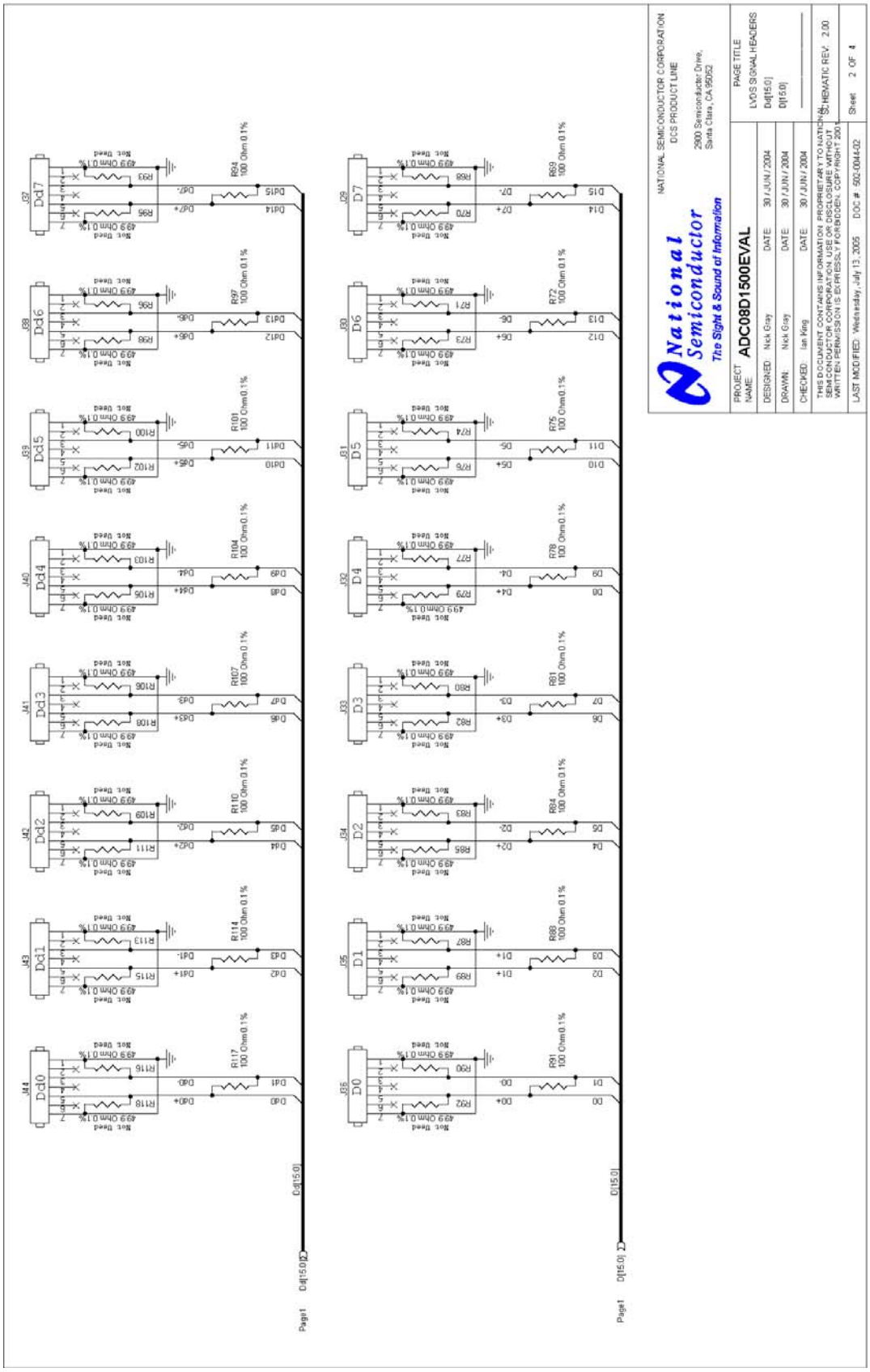
7.0 Evaluation Board Specifications

Board Size:	8.0" x 8.0" (20.3 cm x 20.3 cm)
Power Requirements:	+5.0V, 1.2 A
Clock Frequency Range :	200 MHz to 1.5 GHz
Analog Inputs	
Nominal Voltage:	600 mVP-P or 800 mVP-P
Impedance:	50 Ohms

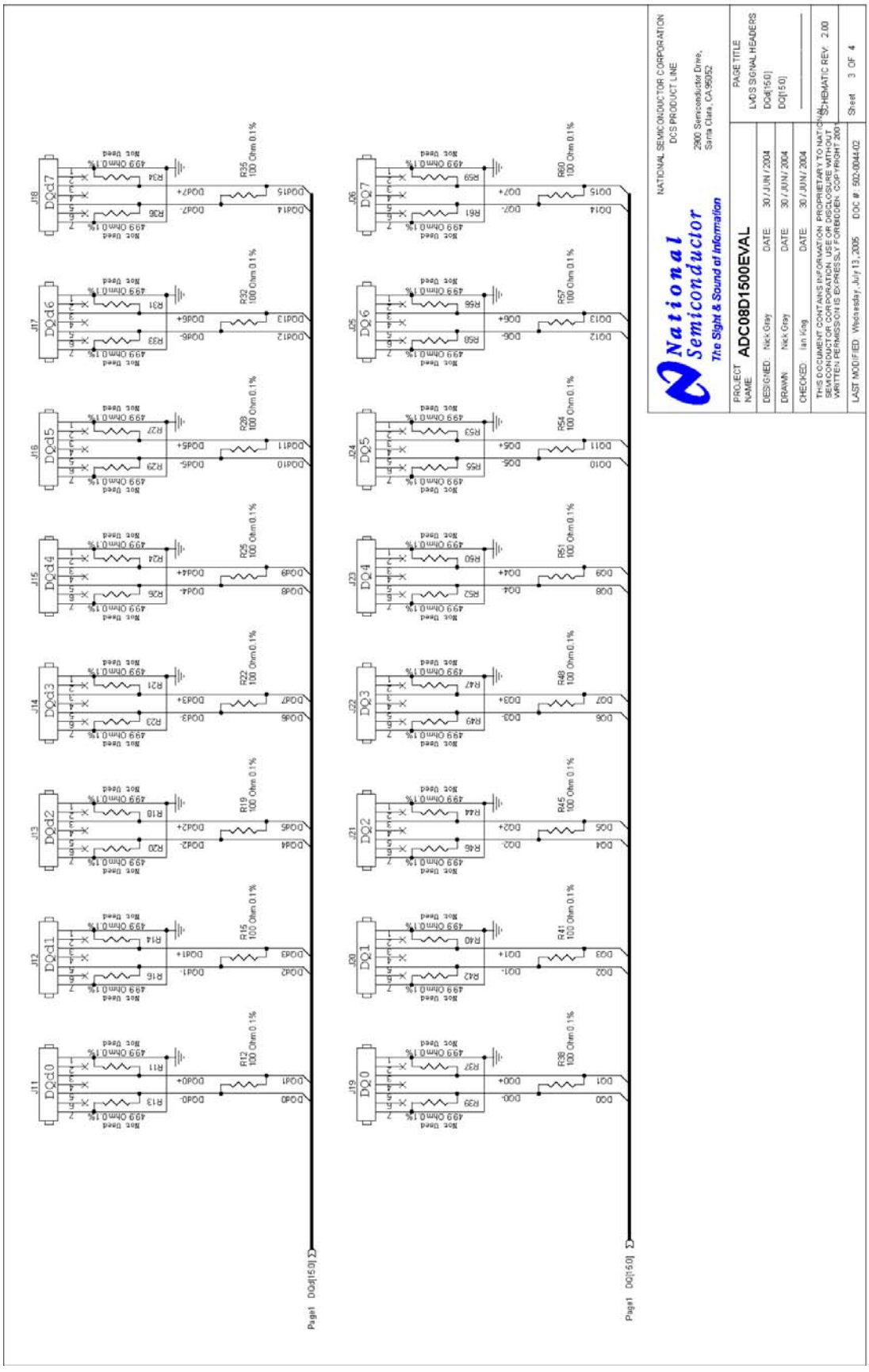
8.0 Schematic Drawing – ADC08D1500EVAL (Page 1 of 4)



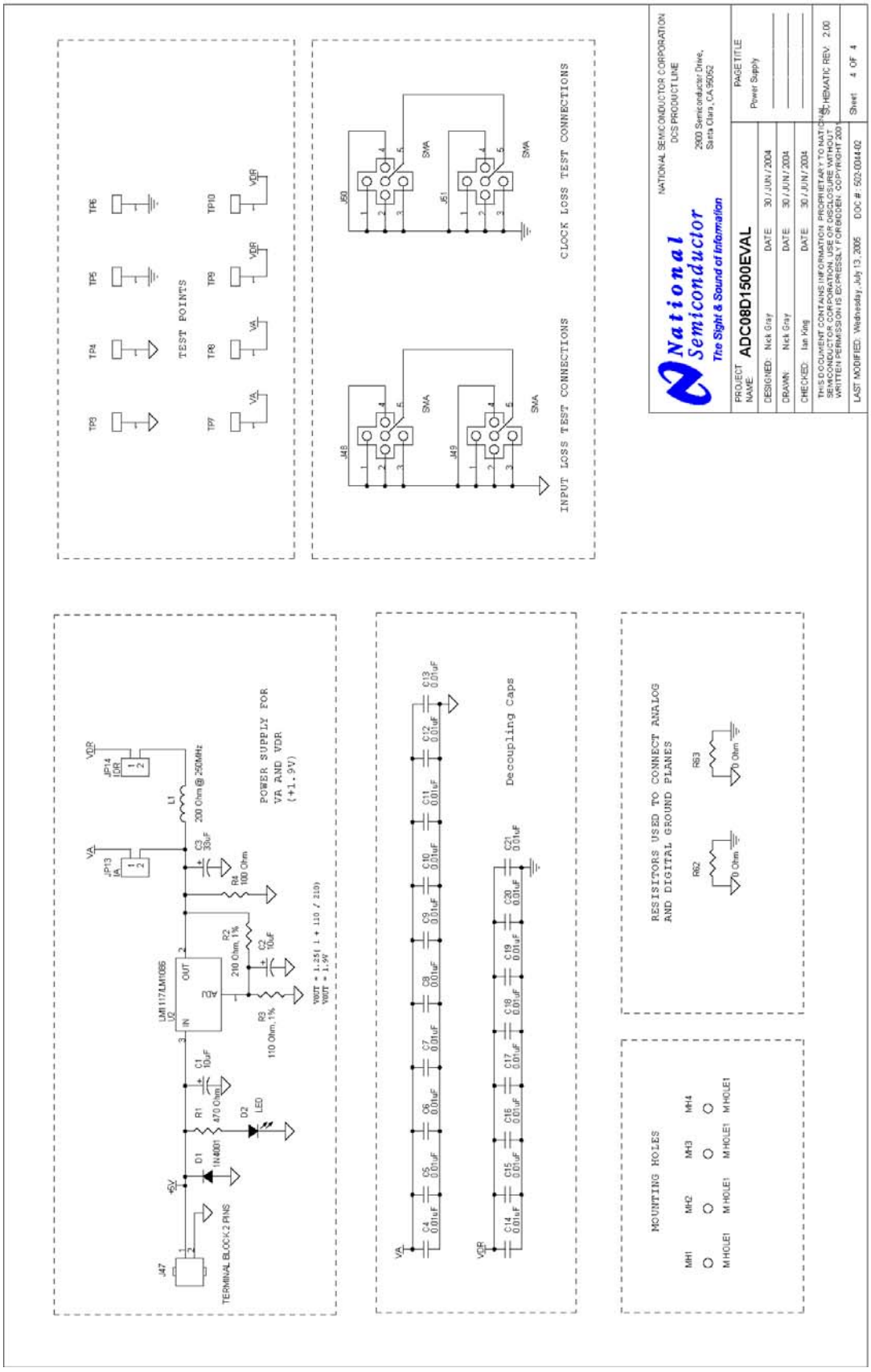
8.1 Schematic Drawing - LVDS Signal Headers (Page 2 of 4)



8.2 Schematic Drawing – LVDS Signal Headers (Page 3 of 4)



8.3 Schematic Drawing – Power Supply (Page 4 of 4)



9.0 Bill of Materials

NSC ADC08D1500 EVALUATION BOARD ASSEMBLY (Rev B)				Release Date: 6/29/2005	
DUAL **BILL Of MATERIALS**					
Item	**Quantity**	**Reference**	**Description**	**MFR**	**MFR P/N**
Capacitors					
1	2	C2,C1	CAP CASE-A TANT 10uF 10V 20%	PANASONIC	ECS-T1AY106R
2	1	C3	CAP CASE-C TANT 33uF 16V 20%	PANASONIC	EEJ-L1CC336R
3	18	C4,C5,C6,C7,C8,C9,C10,	CAP 0603 CERM 0.01uF X7R 16V 10%	PANASONIC	ECJ-1VB1C103K
		C11,C12,C13,C14,C15,C16,			
		C17,C18,C19,C20,C21			
4	3	C23,C24,C31	CAP 0805 CERM 1uF X7R 16V 10%	MURATA	GRM21BR71C105KA01L
5	6	C25,C26,C27,C28,C29,C30	CAP 0805 CERM 0.1uF X7R 16V 10%	PANASONIC	ECJ-2VB1C104K
Diodes					
6	1	D1	RECTIFIER T.H. DO41-AK 1N4001	FAIRCHILD	1N4001
7	2	D2,D6	LED 0805 RED	CHICAGO MINIATURE	CMD17-21VRC/TR8
Connectors					
8	8	JP2,JP3,JP4,JP5,JP6	HEADER 3X1 0.1" SP MALE STR	SULLINS	PTC36SAAN
		JP8,JP12,JP27			
	1	JP1	FIT WIRE LINK 'GND'		
	1	JP10	FIT WIRE LINK 'LVDS'		
	1	JP11	FIT WIRE LINK 'LVDS'		
9	1	JP9	HEADER 5X2 0.1" SP MALE STR	SULLINS	PTC32DAAN
10	3	JP13,JP14,TP1	HEADER 2X1 0.1" SP MALE STR	SULLINS	PTC36SAAN
11	7	J2,J3,J45,J48,J49,J50,J51	CONN SMT SMA 5 PINS 50 OHM	JOHNSON	142-0701-851
12	33	J28,J29,J30,J31,J32,J33	HEADER SMT 7 PINS MALE STR 0.05" PITCH	SAMTEC	FTR-107-03-G-S
		J34,J35,J36,J37,J38,J39			
		J40,J41,J42,J43,J44			
		J11,J12,J13,J14,J15,J16			
		J17,J18,J19,J20,J21,J22			
		J23,J24,J25,J26			
13	1	J47	TERMINAL BLOCK T.H. 2 PINS 0.2" SP	ON SHORE TECH	ED120/2DS
27	5	TP2,TP3,TP7,TP11,TP12	HEADER 1 PIN 0.1" SP MALE STR	SULLINS	PTC36SAAN
Inductors and Transformers					
14	1	L1	CHOKE T.H. WIDE BAND 2.5 TURNS 200 Ohm @ 250MHz	JW MILLER	FB20010-3B
28	3	T1,T2,T3	RF TRANSFORMER SMT 6 PINS upto 1.8GHz	Minicircuits	ADTL2-18
Resisitors					
16	1	R1	RES 0805 470 OHM 1/8W 1%	YAGEO	9C08052A4700FKHFT
17	1	R3	RES 0805 110 OHM 1/8W 1%	PANASONIC	ERJ-6ENF1100V
18	1	R2	RES 0805 210 OHM 1/8W 1%	PANASONIC	ERJ-6ENF2100V
19	1	R4	RES 0805 100 OHM 1/8W 1%	PANASONIC	ERJ-6ENF1000V
20	1	R135	RES 0805 10K OHM 1/8W 1%	PANASONIC	ERJ-6ENF1002V
21	1	R6	RES 0805 3.3K OHM 1/8W 0.1%	PANASONIC	ERA-6YEB332V
22	33	R66,R69,R72,R75,R78,R81	RES 0603 100 OHM 1/10W 0.1%	PANASONIC	ERA-3YEB101V
		R84,R88,R91,R94,R97,R101			
		R104,R107,R110,R114,R117			
		R12,R15,R19,R22,R25,R28			
		R32,R35,R38,R41,R45,R48			
		R51,R54,R57,R60			
23	5	R62,R63,R128,R134,R138	RES 0805 0 OHM 1/8W 5%	PANASONIC	ERJ-6GEY0R00V
24	1	R121	RES 0805 220 OHM 1/8W 0.1%	PANASONIC	ERA-6YEB221V
25	5	R127,R130,R133,R137,R140	RES 0805 100 OHM 1/8W 0.1%	PANASONIC	ERA-6YEB101V
36	2	R5,R10	RES 0805 1K OHM 1/10W 5%		
ICS					
29	1	U1	IC LQFP128 0.5MM PITCH W/ XPAD A/D CONVERTOR	NATIONAL SEMI	ADC08D1500
30	1	U2	IC TO263AB/D2PAK POWER REGULATOR LM1086 1.9V	NATIONAL SEMI	LM1086
31	1	U3	IC SO8 Dual CMOS Differential Line Receiver 3v LVDS	NATIONAL SEMI	DS90LV028A
32	1	U4	IC SOT-23-5 Ultra Low Dropout CMOS Voltage Regulator 150mA	NATIONAL SEMI	LP3985
Misc					
26	1	SW1	SWITCH T.H. MOM TACT 2 PINS 130GF	ITT	PTS635SL43

10.0 Appendix A - Tables of Test Points and Connectors

Table 1 Test Points on the ADC08D1500 Evaluation Board

Test Point	Description
TP 1	VCMO - Common Mode Output Voltage
TP 2	VBG - ADC08D1500 internal band gap voltage
TP 3	Ground
TP 4	Ground
TP 5	Ground
TP 6	Ground
TP 7	VA - ADC08D1500 analog supply voltage
TP 8	VA - ADC08D1500 analog supply voltage
TP 9	VDR - ADC08D1500 output driver supply voltage
TP 10	VDR - ADC08D1500 output driver supply voltage
TP11	Out of Range Signal

Table 2 Power Supply Connections

J47-1	+V	Positive Power Supply (+5V) – Use 4.5V Nominal Input
J47-2	GND	Power Supply Ground

Table 3 Jumper Settings

Jumper Ref	Description	Default Setting
JP1	GROUND	Hard Wired [GND]
JP 2	Digital Output Voltage level (OUTV) - Hi / Low	Hi [1-2]
JP 3	Out Edge, Selects clock edge on which data changes – Positive / Negative	Neg [2-3]
JP 4*	Full Scale Range (FSR) 800mV / 600mV	800mV [1-2]
JP 5**	DCLK_RESET (Active high) Wired to GROUND	Wired [DIFF]
JP 6	ADC (I Channel) Power Down (PD) / Active	Active [2-3]
JP 7	NOT USED	
JP 8	Calibration Delay Short (~17ms) [Lo]/ Long (~1s) [Hi] (Measured @ 1GSPS)	Lo (ms) [1-2]
JP 10	Out of Range Select	Hard Wired [LVDS]
JP 11	Out of Range Select	Hard Wired [LVDS]
JP 12	ADC (Q Channel) Power Down (PD) / Qactive	Qactive[2-3]
JP13	VA Voltage Isolator (Analog Supply)	SHORT (Hard Wired)
JP14	VDR Voltage Isolator (Output Driver Supply)	SHORT (Hard Wired)
JP27	Connection for Temperature Diode	OPEN

NOTE
*JP4 is incorrectly labeled on the PCB. For the Dual ADC it controls the Full Scale Range (FSR)
**JP5 is incorrectly labeled on the PCB. For the Dual ADC pin2 is the DCLK_RST input to the ADC08D1500.

11.0 Appendix B -Evaluating Logic Analyzer Data with WaveVision4 Software

This evaluation board is a stand-alone board and is not intended to directly connect to a data capture board.

Data is captured with a logic analyzer and may be loaded into WaveVision 4 software as described here.

To load a data file captured by a logic analyzer into WaveVision, the data file should be of the following format

1) Contain ASCII text (decimal, octal, hexadecimal or binary radix)

2a) Contain single column data with one data point per line

Or

2b) Contain two data columns separated with a non-numeric character such as a space or comma.

Each column in 2b above should have one data point per line and be from one of the two 8 bit buses for the channel being sampled

Upon opening the file in WaveVision4 (File Menu – Open), a dialog box like the one on the left below will be displayed. For the two-column data here, the delimiter is a space, so the "space" box is shown checked in the dialog box of Figure A2-1, below.

Since the first 8 lines are Logic Analyzer header information, we want to strip them from the data, so "8" is entered in the "Skip Header" information near the bottom of the dialog box of Figure A2-2, below.

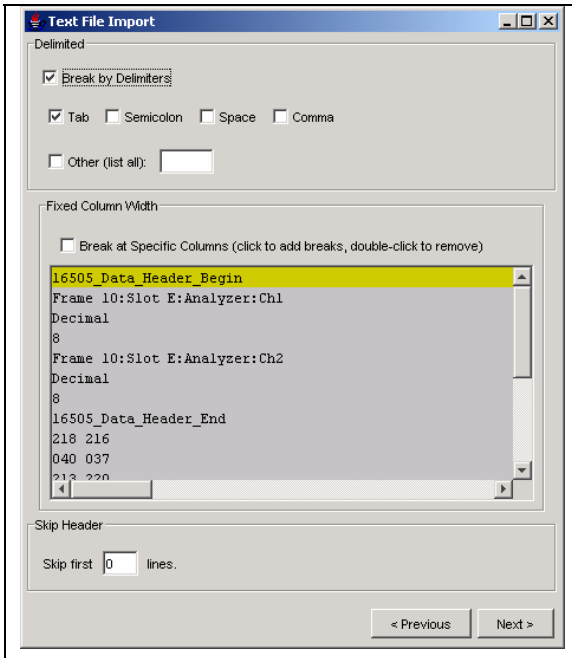


Figure A2-1

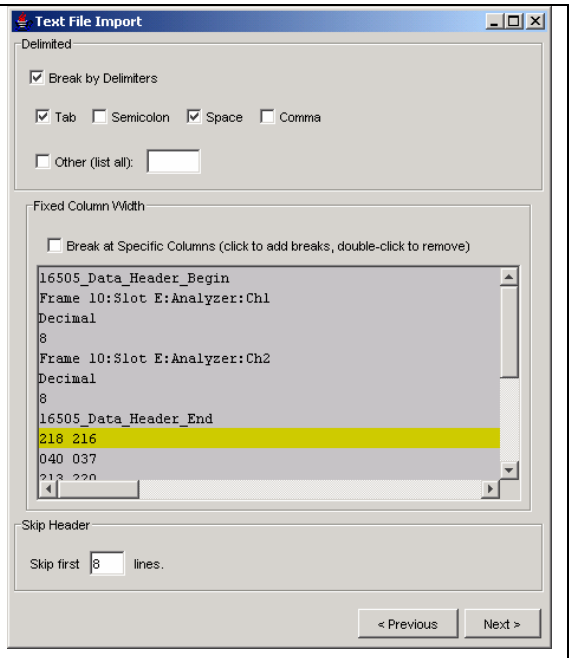


Figure A2-2

The next dialog box shows the two columns with the data points. This data consists of data samples from the ADC, so the "Samples" radio button is checked, as shown in Figure A2-3.

If you wish to re-integrate these two sample sets, click and drag across the two columns. It is not necessary to select all cells of both columns. Figure A2-4 shows both columns selected. These two data sets will be re-integrated, taking 1st data point from Column 1, then 1st data point from column 2, then 2nd data point from Column 1, then 2nd data point from column 2, etc.

If it is desired to swap the columns, that can be done with the final dialog box.

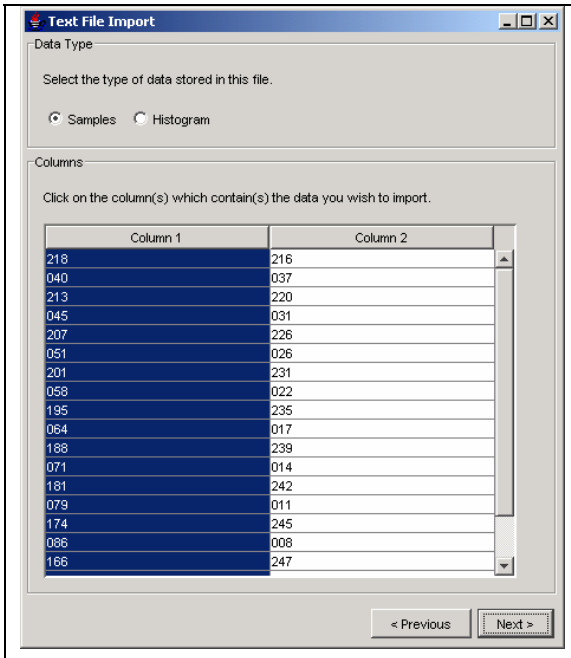


Figure A2-3

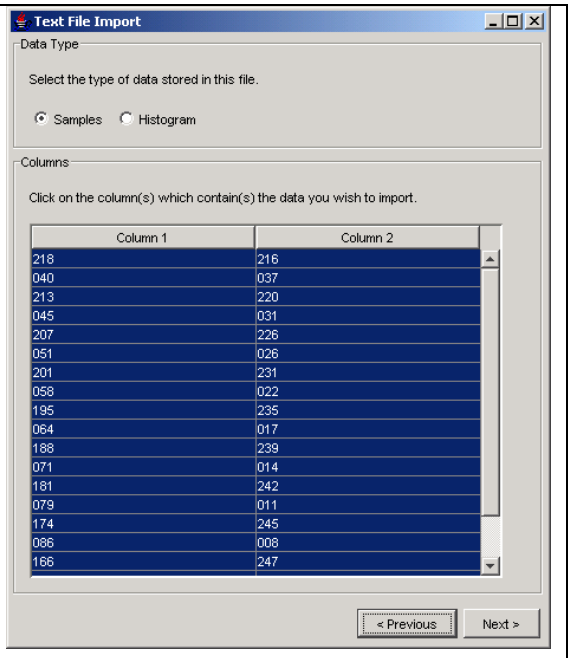


Figure A2-4

The final dialog box is shown in Figure A2-5.

Select the data format (decimal, octal, hexadecimal or binary) with the first pull-down menu.

Enter the sample rate for the data in MHz into the open box.

With the second pull-down menu select the data format (binary, offset binary or two's complement).

To reverse the order in which the data is re-integrated, click and hold one of the column indicators in the "Data" area and drag it to the desired position.

An example of a completed dialog box is shown in Figure A2-6.

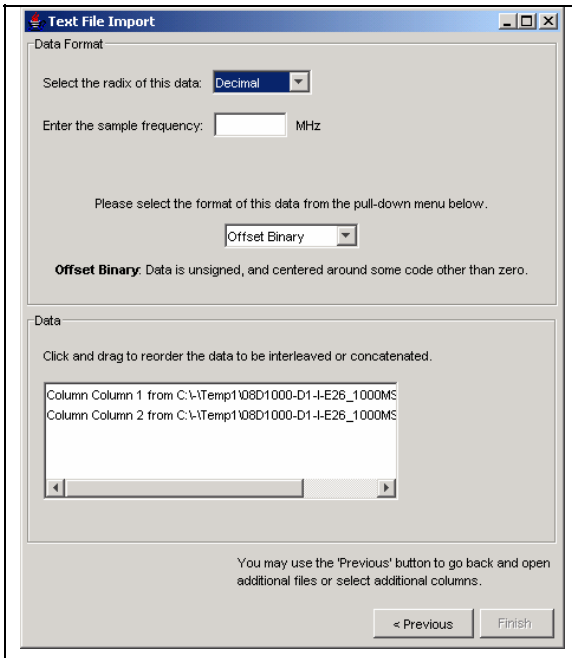


Figure A2-5

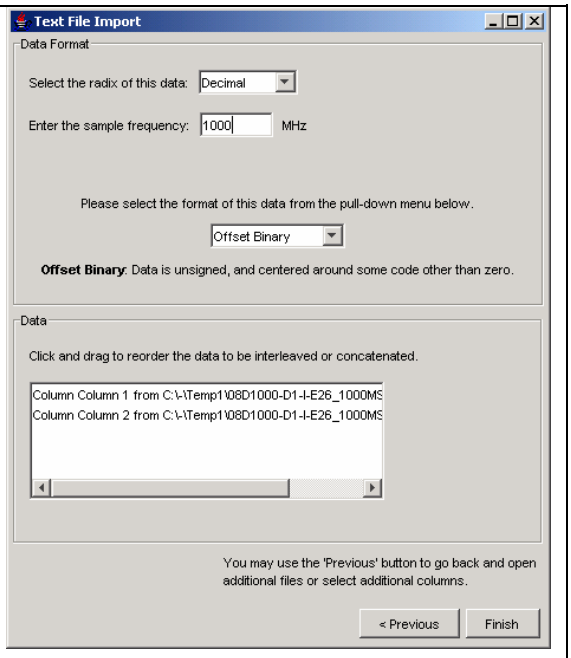


Figure A2-6

The data may now be analyzed in the normal manner. See the WaveVision4 manual for more information.

12.0 Appendix C – Setting up the USI board with Wavevision 4

The Synchronous Serial Port of the ADC08D1500 on the Evaluation Board is brought out to connector J9 shown below in Figure C1.

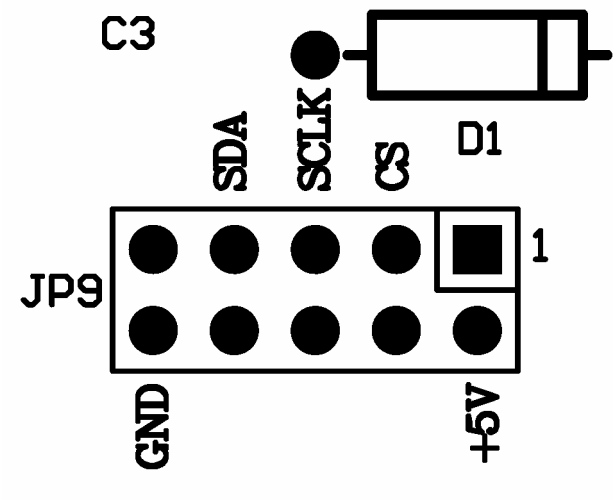


Figure C1

This Header connects directly to the USI board, which is included with the ADC08D1500EVAL kit.

The USI (USB to Serial Interface) board is shown below and connects the host PC to the ADC08D1500EVAL board over a USB interface. Connector JP9 of the USI is connected to JP9 of the ADC08D1500 board with the supplied 3" Ribbon Cable.

IMPORTANT NOTE : PLEASE ENSURE THAT THE WAVEVISION 4 SOFTWARE (version 4.7.1) HAS BEEN FULLY INSTALLED ON TO THE HOST PC BEFORE CONNECTING THE USI TO THE USB PORT OF THE COMPUTER.

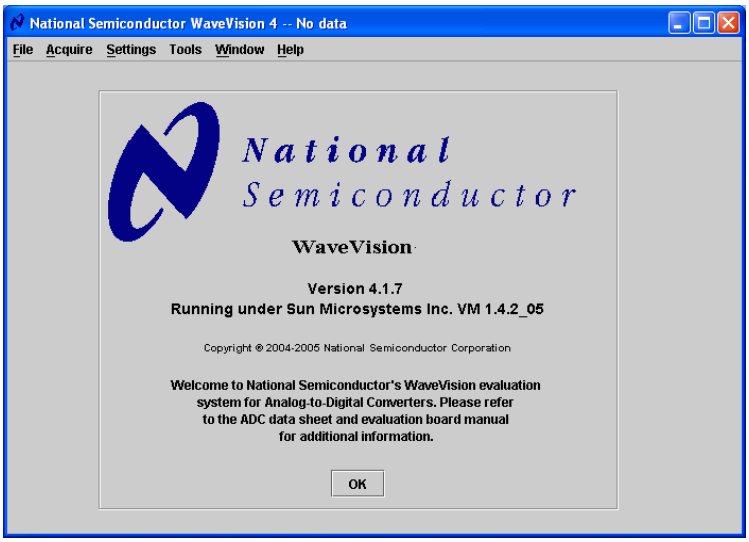
CONNECTING THE USI BEFORE INSTALLING THE CORRECT SOFTWARE MAY RESULT IN THE BOARD BEING REGISTERED AS AN UNKNOWN USB DEVICE. IF THIS HAPPENS YOU WILL NEED TO UNINSTALL THE DEVICE USING THE WINDOWS DEVICE MANAGER BEFORE INSTALLING THE WAVEVISION SOFTWARE

13.0 Appendix D - Installing and running the Wavevision 4 software

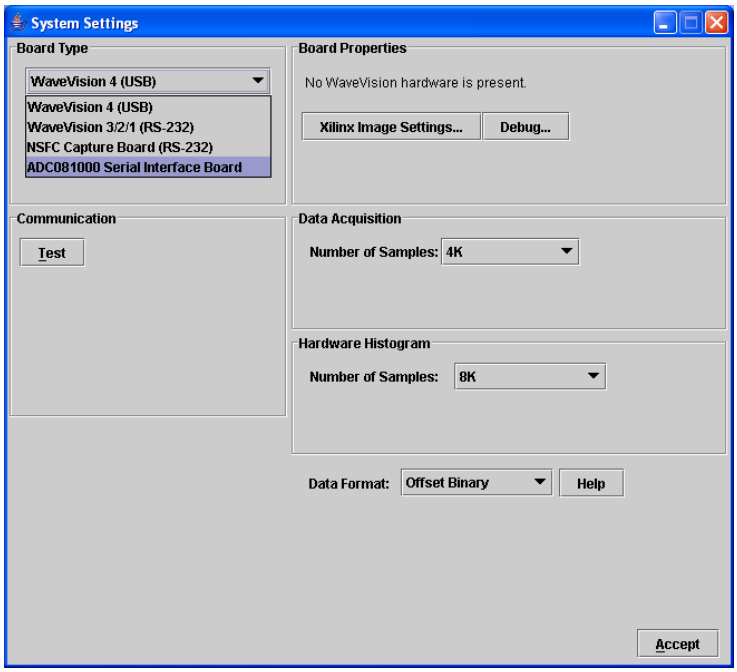
To be able to program the registers of the ADC08D500 using the USI board, the Wavevision software (Version 4.7.1 or later) must be installed on the host PC. This software is supplied on CDROM with the ADC08D1500EVAL board kit, or can be downloaded from the National Website at the following address:

http://www.national.com/appinfo/adc/wv4.html

Follow the on-screen instructions to install the software then launch the application.
The software make take several seconds to initialize, but should display the following welcome screen



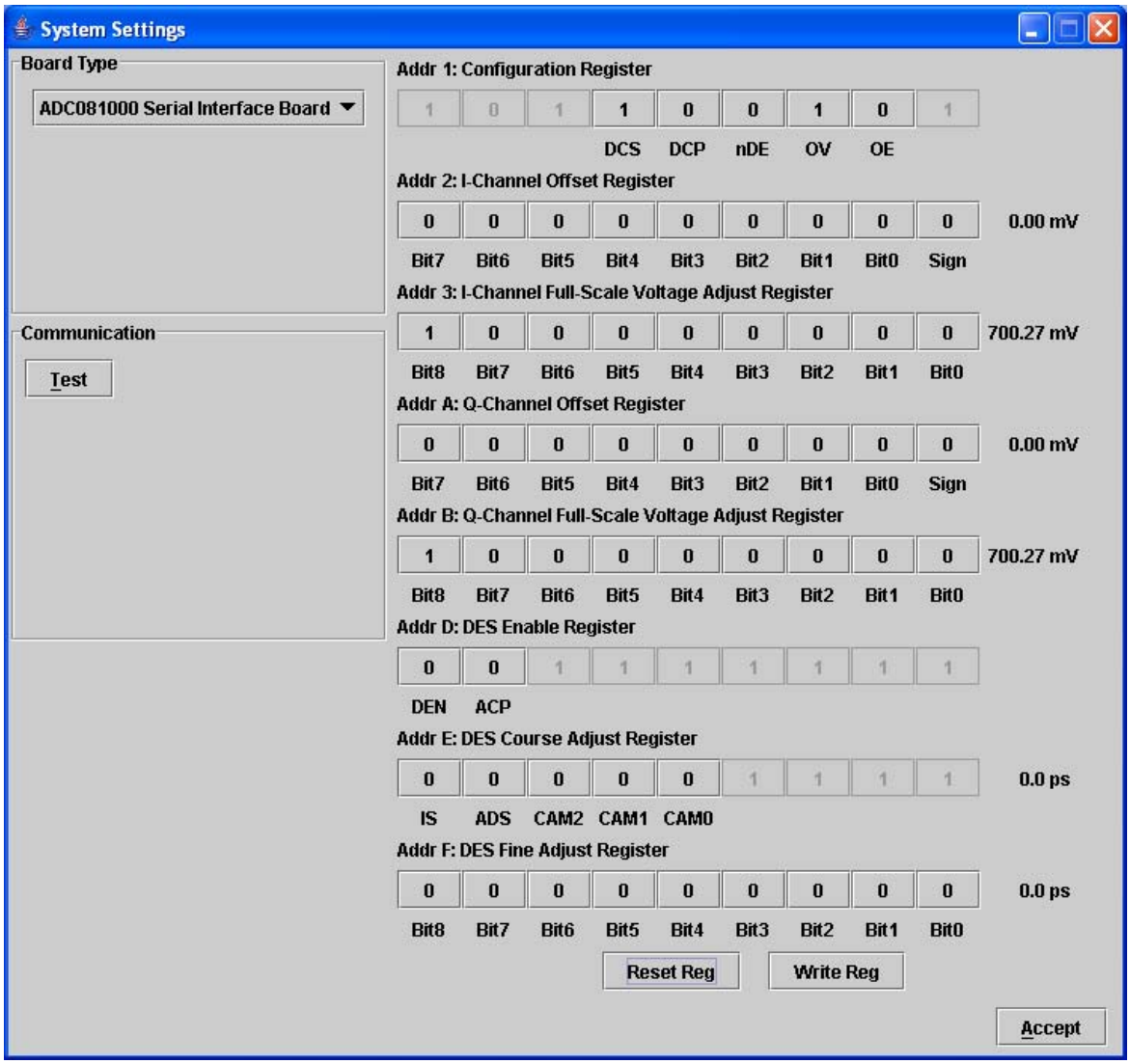
Click on the **Settings** pull down menu and select **Capture Board Settings…**
A window like the one shown below should appear



Click on the **Board Type** selection box in the top left corner and drag the cursor down until the **ADC08D1000 Serial Interface Board** is highlighted.

The Window should then change to show the ADC08D1xxx registers as shown below

NOTE: The registers in the ADC08D1500 are exactly the same as for the lower speed ADC08D1000.



Once this window has opened the USI board can be connected to the PC using the supplied USB cable. Connecting the cable should automatically download the USI firmware to the board.

Click the **Test** button in the communication window and a **Communication successful** Message should appear if all is OK. If communication fails then unplug the USI from the USB cable and then reconnect.

As the ADC08D1500 is a low voltage device, ensure that Jumper J10 on the USI board is set to the 1.8V I/O Voltage option before commencing to program the registers. The green LED (LED1) on the USI board should be off if a 1.8V signaling voltage is selected.

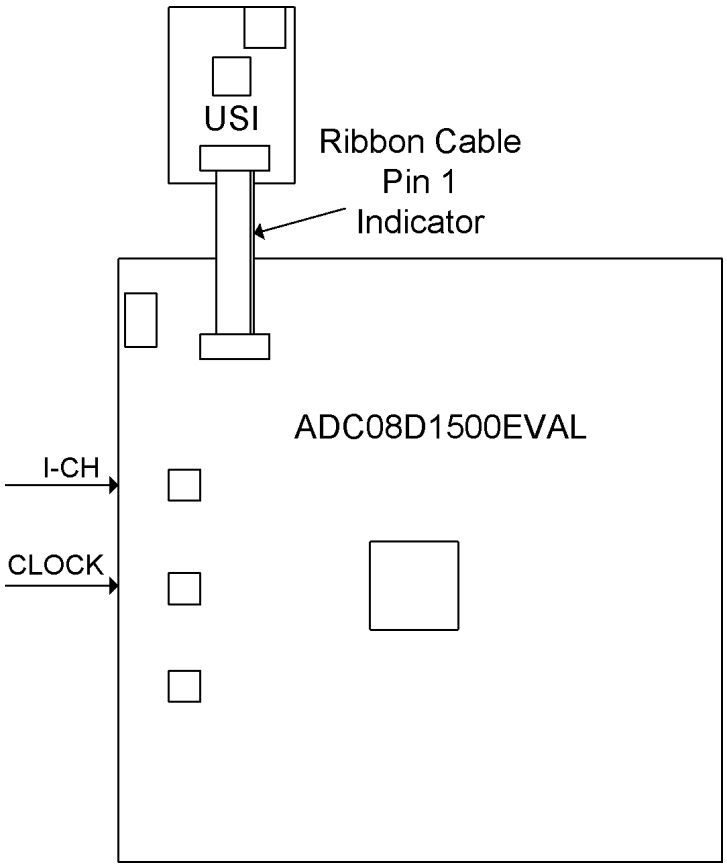
14.0 Appendix E – Configuring the ADC08D1500 for Serial Interface Mode

To enable the serial interface mode, there are four jumper settings that should be assigned as shown in table D1 below

Remove Jumpers JP2, JP3, JP4 and JP8. The centre pins of these jumpers should be floating.

Jumper REF	Description **[SERIAL CONTROL MODE]**	POSITION
JP2	OutV / **[SERIAL CLOCK]**	Remove [Float Pin]
JP3	OutEdge / **[SERIAL DATA]**	Remove [Float Pin]
JP4	FSR / **[Extended Control Enable]**	Remove [Float Pin]
JP8	CalDly / **[Chip Select]**	Remove [Float Pin]

Once the jumpers have been removed, the USI board can be connected to **JP9** of the ADC08D1500 Eval Board as shown in the diagram below.



15.0 Appendix F – Using the Wavevision USI application software

With the ADC08D1500 setup for Extended Control mode as previously detailed, powered on and with the USI board connected, the serial registers of the device are ready for programming.

Please note that the registers of the ADC08D1500 have write capability only. It is not possible to read back the status of any of the internal registers.

The ADC08D1000 register window displayed by the Wavevision 4 software enables the user to select the required state of each individual bit within a particular register.

Clicking a bit will invert the display setting only, it will not perform any register writes until the **Write Reg** button at the bottom of the register window has been clicked.

If a register is updated that relates to a variable such as offset or full scale range, then the absolute value will also be updated on the right side of the window.

The register values can be reset to the default values by clicking on the **Reset Reg** button.
The **Write Reg** button must then be clicked to copy the default values seen on screen into the ADC's registers.

If the Register window is closed by clicking the **Accept** button then the register settings are stored and will be retrieved when the window is opened again. This is useful if the registers need to be reprogrammed to the same state after the ADC and application software have been shutdown.

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